

## DATA SHEET

**NEC**  
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

 $\mu$ PD43256A (F)

## 256K-BIT CMOS STATIC RAM

## DESCRIPTION

The  $\mu$ PD43256A is a high speed, low power, 32K words by 8 bits CMOS static RAM fabricated with advanced silicon-gate CMOS technology. The  $\mu$ PD43256A is low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuitry technique makes the device a high speed and low operating power device which requires no clock or refreshing to operate.

Minimum standby power is drawn by this device when  $\overline{CS}$  is at high level, independently of the other inputs level.

Data retention is guaranteed at a power supply voltage as low 2 volts.

The  $\mu$ PD43256A(F) is Extended-Temperature-Version ( $T_a = -40$  to  $+85$ ).

The  $\mu$ PD43256A(F) is packed in 28-pin DIP, 28-pin SOP.

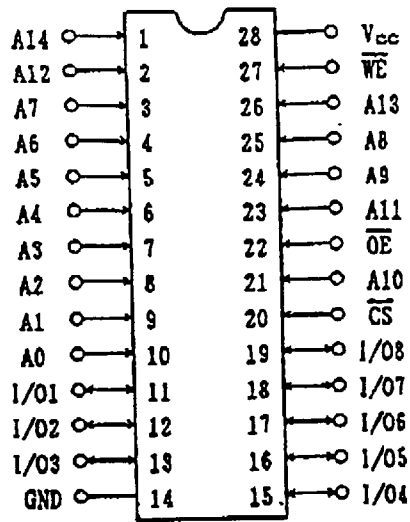
## FEATURES

- 32786 words by 8 bits organization
- Fast Access Time
  - $\mu$ PD43256A(F)-10/10L----100 ns MAX.
  - $\mu$ PD43256A(F)-12/12L----120 ns MAX.
  - $\mu$ PD43256A(F)-15/15L----150 ns MAX.
- Low Power Dissipation (L-Version)
  - Standby Supply Current-----L-Version : 200  $\mu$ A MAX.
  - Data Retention Supply Current---L-Version---15  $\mu$ A MAX- ( $T_a = 0$  to  $40^\circ\text{C}$ )
- Extended Temperature Range:  $T_a = -40$  to  $85^\circ\text{C}$
- Single +5V Supply
- Fully Static Operation: No clock or Refreshing required
- TTL Compatible: All Inputs and Outputs
- Common I/O Using Three-State Output
- One Chip Select and One Output Enable Inputs for Easy Application

## ORDERING INFORMATION

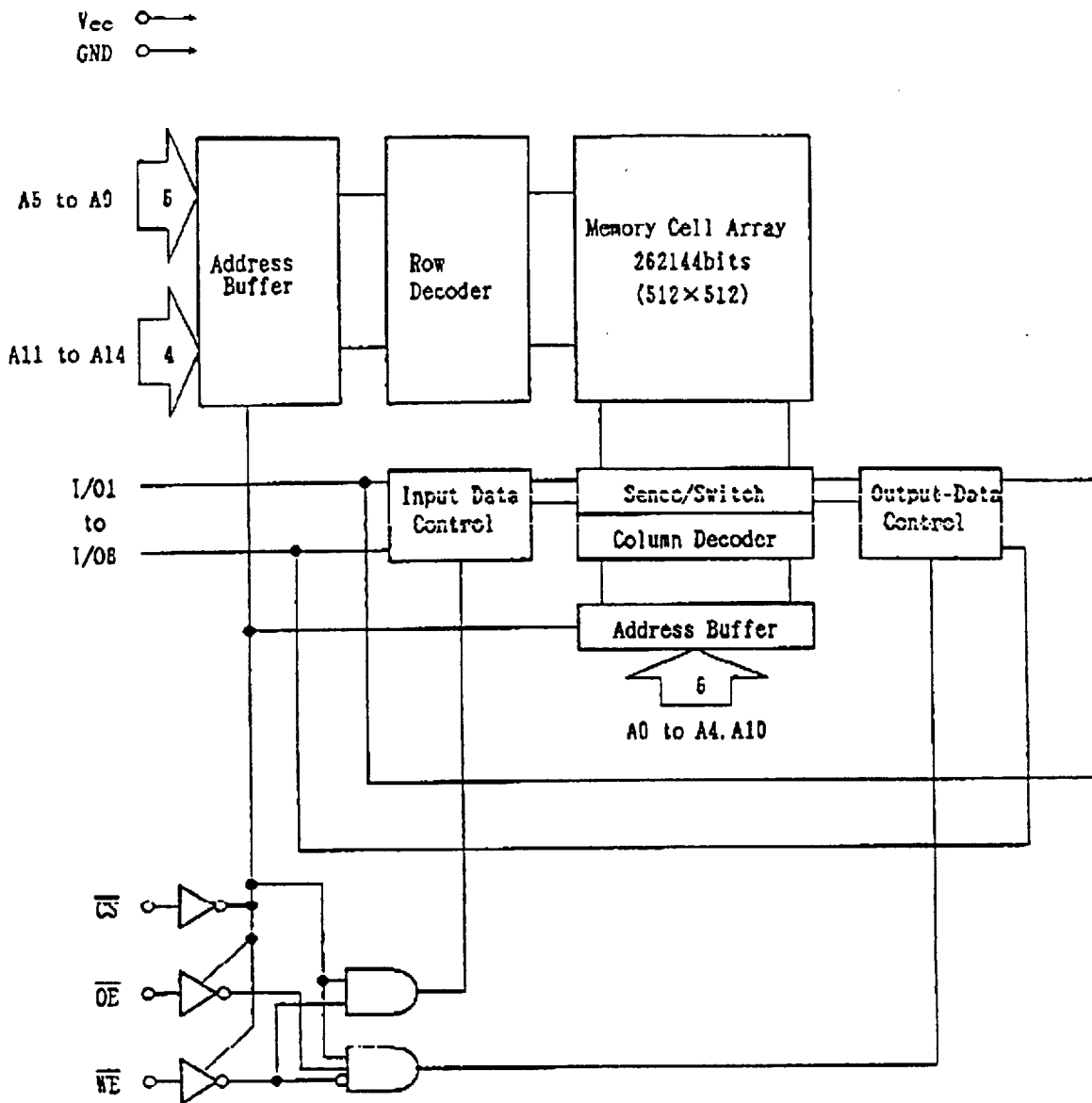
PART NUMBER	PACKAGE	ACCESS TIME(MAX.)	NOTE
MPD43256AC(F)-10	28-pin Plastic DIP(600mil)	100ns	
MPD43256AC(F)-12	"	120ns	
MPD43256AC(F)-15	"	150ns	
MPD43256AC(F)-10L	"	100ns	L-Version
MPD43256AC(F)-12L	"	120ns	"
MPD43256AC(F)-15L	"	150ns	"
MPD43256AGU(F)-10L	28-pin Plastic SOP	100ns	L-Version
MPD43256AGU(F)-12L	"	120ns	"
MPD43256AGU(F)-15L	"	150ns	"

## PIN CONFIGURATION

28-pin Plastic DIP/SOP  
(TOP VIEW)

A0 to A14 : Address input  
 I/O1 to I/O8 : Data input/Output  
 $\overline{CS}$  : Chip Select input  
 $\overline{WE}$  : Write Enable Input  
 $\overline{OE}$  : Output Enable Input  
 V<sub>cc</sub> : Power Supply (+5 V)  
 GND : Ground  
 NC : No Connection

BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	$I_{CC}$
H	X	X	Not Selected	Hi-Z	$I_{SS}$
L	H	H	Output Disable		$I_{COA}$
L	L	H	Read	$D_{OUT}$	
L	X	L	Write	$D_{IN}$	

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Supply Voltage	$V_{CC}$		-0.5 <sup>Note 1</sup> to +7.0	V
Input/Output Voltage	$V_I$		-0.5 <sup>Note 1</sup> to $V_{CC}+0.5$	V
Operating Temperature	$V_{OP}$		-40 to +85	°C
Storage Temperature	$V_{STG}$		-55 to +125	°C

Note: -3.0V MIN. (Pulse Width 50ns)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage $V_{CC}$	$V_{CC}$		4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$		2.4		$V_{CC}+0.5$	V
Input Low Voltage	$V_{IL}$		-0.3 <sup>Note 1</sup>		0.6	V
Ambient Temperature	$T_a$		-40		85	°C

Note: -3.0V MIN. (Pulse Width 50ns)

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	$\mu PD43256A(F)$			$\mu PD43256A(F)-L$			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Leakage Current	$I_{IL}$	$V_{IH}=0$ V to $V_{CC}$	-1.0		1.0	-1.0		1.0	$\mu A$
I/O Leakage Current	$I_{LO}$	$V_{I/O}=0$ V to $V_{CC}$ $\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$	-1.0		1.0	-1.0		1.0	$\mu A$
Operating Supply Current	$I_{CC(A)}$	$\overline{CS}=V_{IL}$ MIN. Cycle $I_{I/O}=0$ mA	$\mu PD43256A(F)$ -10		60			40	mA
			$\mu PD43256A(F)$ -12		40			40	mA
			$\mu PD43256A(F)$ -15		35			35	mA
	$I_{CC(B)}$	$\overline{CS}=V_{IL}$ , $I_{I/O}=0$ mA			15			15	mA
$I_{CC(C)}$	$\overline{CS} \leq 0.2V$ , Cycle=1MHz, $I_{I/O}=0$ mA $V_{IL} \leq 0.2V$ , $V_{IH} \geq V_{CC}-0.2V$			15			15	mA	
Standby Supply Current	$I_{SS}$	$\overline{CS}=V_{IH}$			5			3	mA
	$I_{SS1}$	$\overline{CS} \geq V_{CC}-0.2$ V		0.02	2		0.002	0.2	mA
Output High Voltage	$V_{OH1}$	$I_{OH}=1.0$ mA	2.4			2.4			V
	$V_{OH2}$	$I_{OH}=0.1$ mA	$V_{CC}-0.5$			$V_{CC}-0.5$			V
Output Low Voltage	$V_{OL}$	$I_{OL}=2.1$ mA			0.4			0.4	V

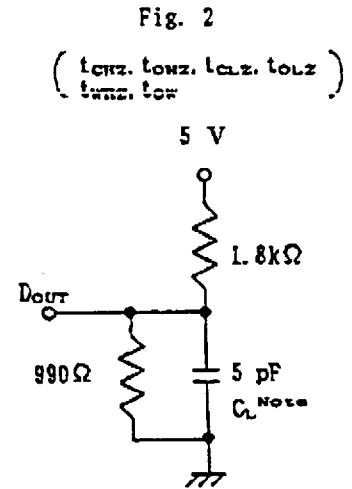
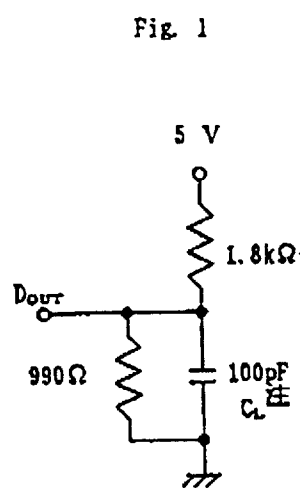
CAPACITANCE (Ta=25 °C, f=1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	單位
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0 V			8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0 V			5	pF

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

AC TEST CONDITIONS

- Input Pulse Levels : 0.5 ~ 2.4 V
- Input Pulse Rise and Fall Time : 5 ns
- Timing Reference Levels : 1.5 V
- Output Load : See Fig. 1.2.

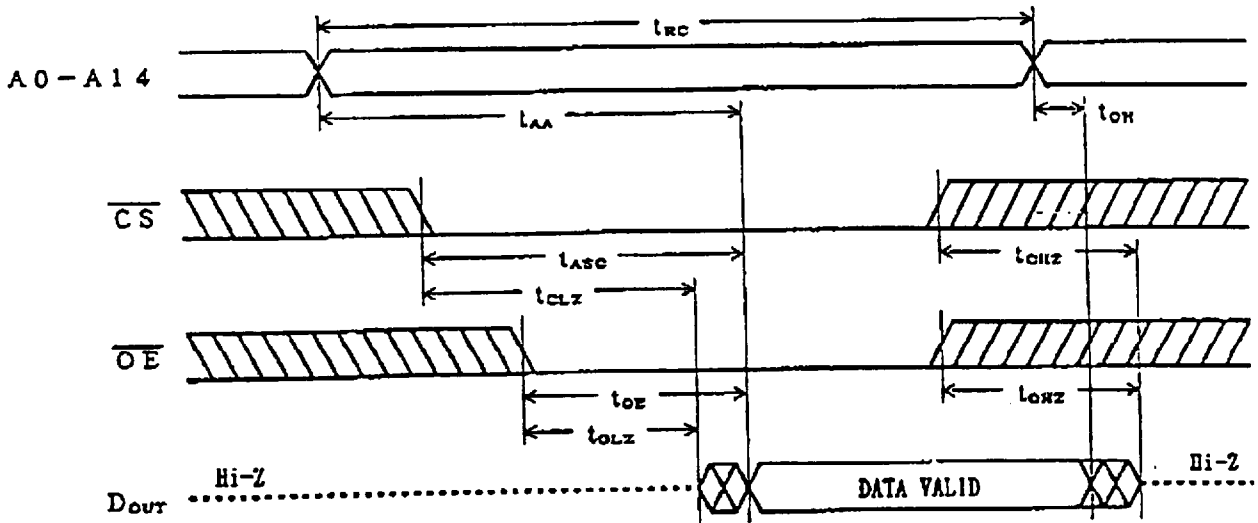


Note: including scope and jig.

READ CYCLE

PARAMETER	SYMBOL	μPD43256A(F) -10		μPD43256A(F) -12		μPD43256A(F) -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>WC</sub>	100		120		150		n s
Address Access Time	t <sub>AA</sub>		100		120		150	n s
Chip Select Access Time	t <sub>ACS</sub>		100		120		150	n s
Output Enable to Output Valid	t <sub>OE</sub>		50		60		70	n s
Output Hold from Address Change	t <sub>OH</sub>	10		10		10		n s
Chip Select to Output in Lo-z	t <sub>CLZ</sub>	10		10		10		n s
Output Enable to Output in Lo-z	t <sub>OLZ</sub>	5		5		5		n s
Chip Select to Output in Hi-z	t <sub>CHZ</sub>		35		40		50	n s
Output Enable to Output in Hi-z	t <sub>OHZ</sub>		35		40		50	n s

READ CYCLE TIMING CHART NOTE1



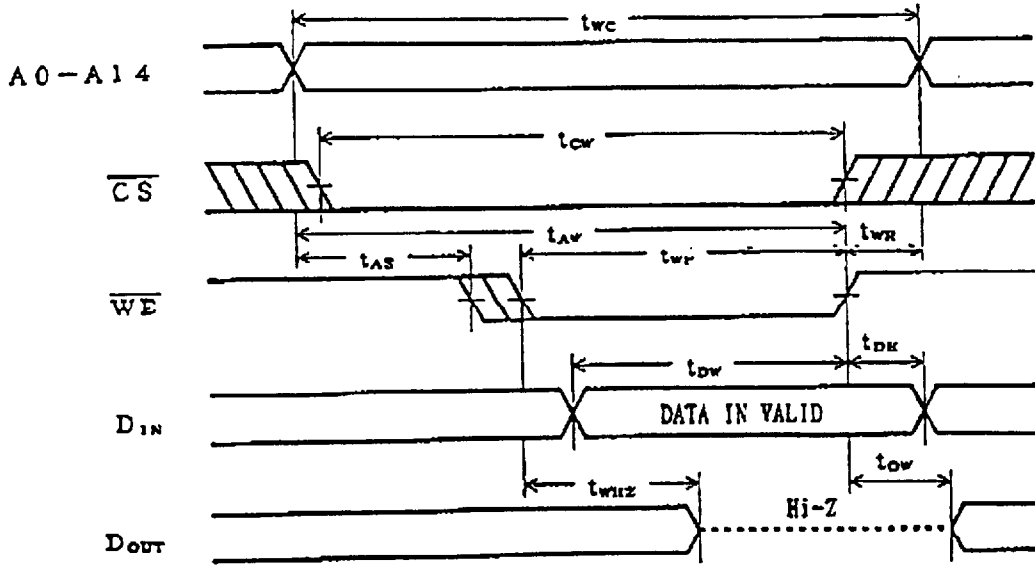
Note 1 :  $\overline{WE}$  is high for read cycle.

WRITE CYCLE

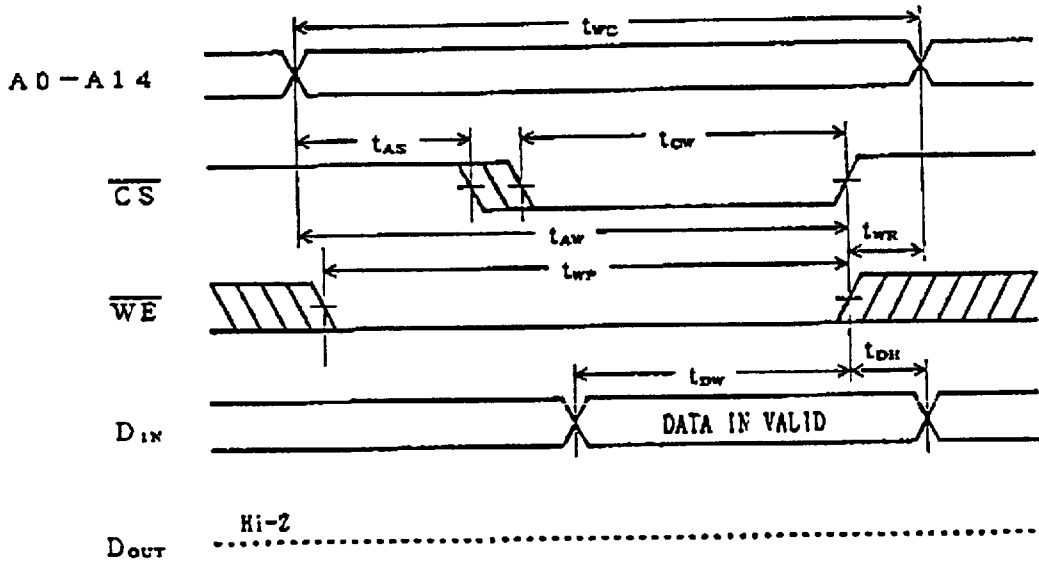
PARAMETER	SYMBOL	$\mu PD43256A(F)$ -10		$\mu PD43256A(F)$ -12		$\mu PD43256A(F)$ -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	$t_{WC}$	100		120		150		n s
Chip Select to end of Write	$t_{CW}$	80		85		100		n s
Address Valid to end of Write	$t_{AW}$	80		85		100		n s
Address Setup Time	$t_{AS}$	0		0		0		n s
Write Pulse Width	$t_{WP}$	70		70		90		n s
Write Recovery Time	$t_{WR}$	10		10		10		n s
Data Valid to end of Write	$t_{DW}$	40		50		60		n s
Data Hold Time	$t_{DH}$	0		0		0		n s
Write Enable to Output in Hi-z	$t_{WEZ}$		35		40		50	n s
Output Active from end of Write	$t_{OW}$	10		10		10		n s

WRITE CYCLE TIMING CHART

WRITE CYCLE ( $\overline{WE}$  CONTROLLED) NOTE 1.2.3



WRITE CYCLE ( $\overline{CS}$  CONTROLLED) NOTE 1.2



NOTE1: A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ .

2:  $\overline{CS}$  or  $\overline{WE}$  must be high during address transition.

3: If  $\overline{OE}$  is high, I/O pins remain in a high impedance state.

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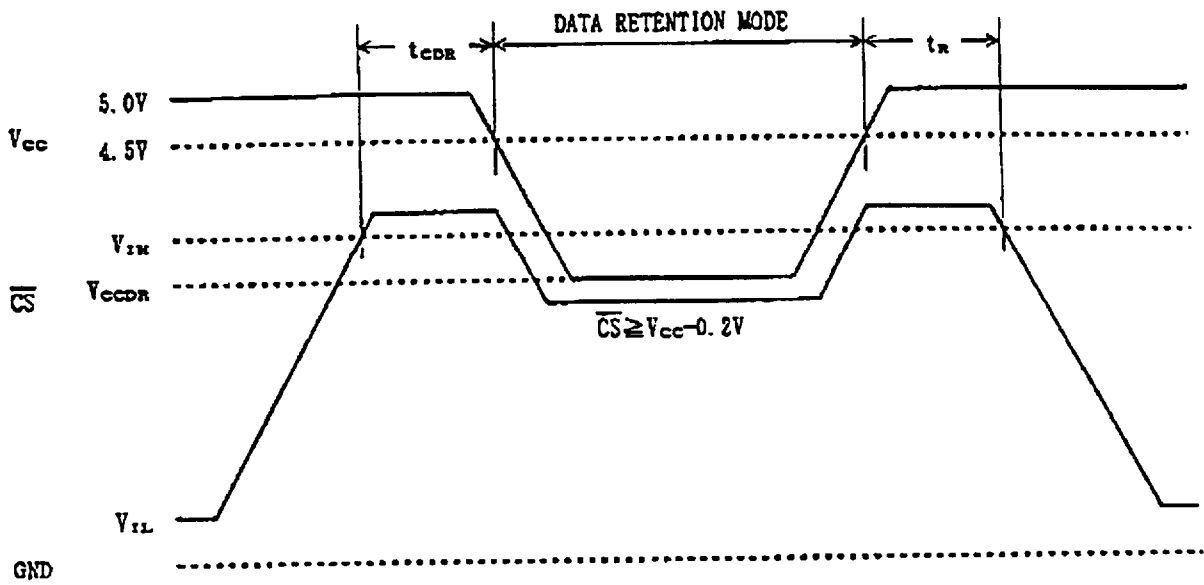


LOW V<sub>CC</sub> DATA RETENTION CHARACTERISTICS (T<sub>a</sub>=-40 to 85°C) L-Version

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V <sub>CCDR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Supply Current	I <sub>CCDR</sub>	V <sub>CC</sub> =3.0V, $\overline{CS} \geq V_{CC} - 0.2V$		1	100 <sup>NOTE</sup>	μA
Chip Deselection to Data Retention Mode	t <sub>CDR</sub>		0			ns
Operation Recovery Time	t <sub>R</sub>		t <sub>RC</sub>			ns

Note T<sub>a</sub>=0 to 40°C : 15μA MAX.

DATA RETENTION TIMING CHART Note 1



Note: The other inputs (Addresses,  $\overline{OE}$ ,  $\overline{WE}$ , I/Os) can be in a high impedance state.